DETAILED ACTION

1. This communication is responsive to Amendment filed 01/28/2010.

2. Claims 1, 3, 5-24 are pending in this application. Claims 1, 11, 17 and 21-22 are independent claims. In Amendment, claims 2 and 4 are cancelled and claims 23-24 are added. This Office Action is made non-final after a RCE filed 01/28/2010.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 3, 5-21 and 23-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Re claim 1, the limitation "DSP ONLY capable of supporting ... number of bits that are fewer in number than.." is not fully support or described in the original specification since the specification does not absolutely mention about the DSP ONLY support the number of bits that are fewer in number than that forming the first and second numbers. Claims 11, 17 and 21 have the same rejection.

Thus, claims 3, 5-10, 12-16, 18-20 and 23-24 are also rejected for being dependent on the rejected base claims 1, 11 and 17.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 3 and 5-21 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the term "capable of" in line 7 is a relative term which renders the claim indefinite. The term "capable of" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3, 5-7, 9 and 11-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhandal et al. (U.S. 6,711,602) in view of Schier et al. (U.S. 7,046,723).

Re claim 1, Bhandal et al. disclose in Figures 1-22 a method for performing multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture of multiplier), comprising: generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. Figure 11B wherein SRC1_L as B is multiplying with SRC2_L as D by B*D) using a digital signal processor (DSP) only capable of supporting multiplication on a number of bits that are fewer in number than that forming the first and second numbers (e.g. Figures 11-12 wherein first and second numbers are considered as the source 1 and source 2 respectively and the multiplication is done on the portion of sources as high portion or lower portion of the source by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands); a product of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11B wherein SRC1_H as A is multiplying with SRC2_H as C by A*C) wherein the second plurality of bits from the first number is fewer than the bits of the first number and the second plurality of bits from the second number is fewer than the bits of the second number (e.g. the number of bits of high or low portion of the source is less than the whole bits of source as seen in Figures 11-12 wherein either high or low portion is only 16 bits compare to 32 bits of the source); scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. by shifter 810 in Figure 8) and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (e.g. by shifter 811

in Figure 8); and summing a scaled product and a scaled stored value to generate a value representing a product of the first number and the second number (e.g. output of adder 820 in Figure 8 and Figure 11B), wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits (e.g. Figure 11B wherein each of input operands consist of 32 bits and each of input multiplied operand is 16 bits).

Bhandal et al. fail to disclose the multiplier is on a field programmable gate array and the second product is retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is on a field programmable gate array (e.g. abstract) and the second product is retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is on a field programmable gate array and the second product is retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 3, Bhandal et al. further disclose in Figures 1-22 the DSP block is configured to multiply two numbers of equal bit length (e.g. 16 bits by 16 bits in Figure 11B).

Re claim 5, Bhandal et al. further disclose in Figures 1-22 scaling the product comprises shifting bits in the product relative to a global least significant bit (e.g. Figures 8 and 11B).

Re claim 6, Bhandal et al. further disclose in Figures 1-22 scaling the stored value comprises shifting bits in the product relative to a global least significant bit (e.g. Figures 8 and 11B).

Re claim 7, Bhandal et al. fail to disclose in Figures 1-22 retrieving a second stored value designated as a product era third plurality of bits from the first number and a third plurality of bits from the second number; retrieving a third gored value designated as a product of a fourth plurality of bits from the first number and a fourth plurality of bits from the second number; scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number and scaling the third stored value with respect to a position of the fourth plurality orbits from the first number and a position of the fourth plurality of bits from the second number, and summing a scaled second stored value and a scaled third stored value. However, Schier et al.'s disclose in Figures 1-4 retrieving a second stored value designated as a product of a third plurality of bits from the first number and a third plurality of bits from the second number (e.g. b2x in Figure 1); retrieving a third gored value designated as a product of a fourth plurality of bits from the first number and a fourth plurality of bits from the second number (e.g. b3x in Figure 1); scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number (e.g. bit shift left in Figures 2-4) and scaling the third stored value with respect to a position of the fourth plurality of bits from the first number and a position of the fourth plurality of bits

from the second number (e.g. bit shift left in Figures 2-4), and summing a scaled second stored value and a scaled third stored value (e.g. output of adder 3 in Figure 1).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to retrieving a second stored value designated as a product era third plurality of bits from the first number and a third plurality of bits from the second number; retrieving a third gored value designated as a product of a fourth plurality of bits from the first number and a fourth plurality of bits from the second number; scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number and scaling the third stored value with respect to a position of the fourth plurality orbits from the first number and a position of the fourth plurality of bits from the second number, and summing a scaled second stored value and a scaled third stored value as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 4 lines 3-21).

Re claim 9, it has similar limitations cited in claim 7. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 11, Bhandal et al. disclose in Figures 1-22 a method for implementing a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture) utilizing a single DSP only capable of supporting multiplication on a fewer number of bits than that forming the first and second numbers (e.g. Figure 11B and Figures 11-12 wherein first and second numbers are considered as the source 1 and source 2 respectively and the multiplication is done on the portion of

sources as high portion or lower portion of the source by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands), comprising: configuring a digital signal processor (DSP) to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. Figure 11B with product B*D) where the first plurality of bits from the first and second numbers are fewer than the bits forming the first and second number (e.g. the number of bits of high or low portion of the source is less than the whole bits of source as seen in Figures 11-12 wherein either high or low portion is only 16 bits compare to 32 bits of the source); products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11B with product A*C) where the second plurality of bits from the first and second numbers are fewer than the bits forming the first and second number (e.g. the number of bits of high or low portion of the source is less than the whole bits of source as seen in Figures 11-12 wherein either high or low portion is only 16 bits compare to 32 bits of the source); routing an output from the DSP to an adder such that the output from the DSP is scaled according to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. by shifter 810 in Figure 8), routing an output as second product to the adder (e.g. adder 820 in Figure 8) such that the output is scaled according to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (e.g. by shifter 811 in Figure 8), and outputting a value representing a product of the second number where the first and second number each have more than the first plurality of bits

(e.g. output of adder 820 in Figure 8), wherein the DSP is configured to support multiplication of no more than the first plurality of bits (e.g. 16 bits by 16 bits).

Bhandal et al. fail to disclose the multiplier is on a field programmable gate array and the second product is stored/retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is on a field programmable gate array (e.g. abstract) and the second product is stored/retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is on a field programmable gate array and the second product is stored/retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 12, it has similar limitations cited in claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, Bhandal et al. further disclose in Figures 1-22 configuring the DSP comprises determining a number of bits that the DSP will multiply (e.g. Figure 11B).

Re claim 14, Bhandal et al. further disclose in Figures 1-22 determining a number of the second plurality of bits from the first number and a number of the second plurality of bits from the second number (e.g. Figure 11B).

Re claim 15, Bhandal et al. further disclose in Figures 1-22 routing the output from the DSP has the effect of shifting the output from the DSP to a more significant bit position (e.g. left shifting 810 in Figure 8).

Re claim 16, Bhandal et al. fail to disclose in Figures 1-22 routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position. However, Schier et al. disclose in Figures 1-4 routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position (e.g. by bit shift left in Figures 2-4).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 17, Bhandal et al. disclose in Figures 1-22 a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture), comprising: a digital signal processor (DSP) only capable of supporting multiplication on a number of bits fewer than that forming the first and second numbers (e.g. Figures 11-12 wherein first and second numbers are considered as the source 1 and source 2 respectively and the multiplication is done on the portion of sources as high portion or lower portion of the source by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands), the DSP configured to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. Figure 11B to produce B*D); a product resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11B to produce A*C) where

the second plurality of bits from the first number is less than the bits forming the first number and the second plurality of bits from the second number is less than the bits forming the second number (e.g. the number of bits of high or low portion of the source is less than the whole bits of source as seen in Figures 11-12 wherein either high or low portion is only 16 bits compare to 32 bits of the source); and an adder that sums (e.g. by adder 820 in Figure 8) a scaled output of the DSP and a scaled output of the second product to output a value representing a product of the first and second number where the first and second number each have more than the first plurality of bits (e.g. by shifters 810 and 811 respectively).

Bhandal et al. fail to disclose the second product is stored/retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the second product is stored/retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the second product is stored/retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 18, Bhandal et al. fail to disclose in Figures 1-22 the DSP, the memory, and the adder reside on a field programmable gate array. However, Schier et al. disclose in Figures 1-4 the DSP, the memory, and the adder reside on a field programmable gate array (e.g. abstract).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the DSP, the memory, and the adder reside on a field programmable gate array as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 19, it has similar limitations cited in claim 7. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 20, Bhandal et al. further disclose in Figures 1-22 the adder sums a sealed output of the second memory with the scaled output of the DSP and the scaled output of the memory (e.g. by adder 820 or adder 3).

Re claim 21, Bhandal et al. disclose in Figures 1-22 a method for implementing a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture), comprising: configuring a digital signal processor (DSP), only capable of supporting multiplication on a number of bits that are fewer than those forming the first and second numbers (e.g. Figures 11-12 wherein first and second numbers are considered as the source 1 and source 2 respectively and the multiplication is done on the portion of sources as high portion or lower portion of the source by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands), to perform multiplication on a first n bits from a first number and a first n bits from a second number (e.g. by product B*D in Figure 11B); products resulting from multiplication of a second m bits from the first number and a second m bits from the second number (e.g. by product A*C in Figure 11B); routing an output from the DSP to

an adder (e.g. adder 820 in Figure 8) such that the output from the DSP is scaled according to a position of the first n bits from the first number and a position of the first n bits from the second number (e.g. by shifter 810 in Figure 8); routing an output of the second product to the adder such that the output from the memory is sealed according to a position of the second m bits from the first number and a position of the second m bits from the second number (e.g. by shifter 811 in Figure 8); and outputting a value representing a product of the first and second number where the first and second number each have at least n + m number of bits (e.g. output of adder 820 in Figure 8 and Figure 11B).

Bhandal et al. fail to disclose the multiplier is on a field programmable gate array and the second product is retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is on a field programmable gate array (e.g. abstract) and the second product is retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is on a field programmable gate array and the second product is retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 22, Bhandal et al. disclose in Figures 1-22 a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture) comprising: a digital signal processor (DSP) configured to perform

n*n multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. produce B*D in Figure 11B with 16x16 bits multiplication); products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. produce A*C in Figure 11B with 16x16 bits multiplication); and an adder that sums a scaled output of the DSP and a scaled (e.g. scaling by shifters 810 and 811 in Figure 8) output of the memory to output a value representing a product of the first and second number (e.g. by adder 820 in Figure 8) where the first and second number each have more than n bits (e.g. each have 32 bits or 2n total in Figure 11B).

Bhandal et al. fail to disclose the second product is stored/retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the second product is stored/retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the second product is stored/retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 23, Bhandal et al. further disclose in Figures 1-22 scaling the product comprising routing the product directly to an adder at inputs of appropriate significance (e.g. by shifter 810 in Figure 8 as an example in Figure 11B by shifting down the upper portion).

Re claim 24, Bhandal et al. further disclose in Figures 1-22 scaling the stored value comprises routing the stored value directly to an adder at inputs of appropriate significance (e.g. by shifter 810 in Figure 8 as an example in Figure 11B by shifting down the upper portion).

Allowable Subject Matter

9. Claims 8 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

10. The amendment filed 01/28/2010 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

The limitation "DSP ONLY capable of supporting ... number of bits that are fewer in number than.." in independent claims 1, 11, 17 and 21 is not fully support or described in the original specification since the specification does not absolutely mention about the DSP ONLY support the number of bits that are fewer in number than that forming the first and second numbers.

Applicant is required to cancel or clearly point the support language of the new matter in the reply to this Office Action.

Response to Arguments

11. Applicant's arguments filed 01/28/2010 have been fully considered but they are not persuasive.

a. The applicant argues in pages 10-11 for claims that the cited reference by Bhandal and Schier do not disclose the amended claims, particularly the added limitations since DSP in Bhandal is capable of supporting multiplication on all the bits forming the first and second numbers.

The examiner respectfully submits that the above rejection fully addresses all the limitations in the claims, particularly the newly added limitations wherein the number of bits of high or low portion of the source is less than the whole bits of source as seen in Figures 11-12 wherein either high or low portion is only 16 bits compare to 32 bits of the source. Generally, Figures 11 show multiple way of performing multiplications wherein the multipliers and multiplicands are less then the sources or the first and second numbers as cited in the claimed invention. For instant, Figure 11B show first numbers as 32-bits source 1 and second numbers as 32-bits source 2 and the multiplication is performed on either lower or upper portion of the first and second numbers to produce AC and/or BD. Thus, clearly DSP is capable of supporting multiplication on a number of bits that are fewer in number than that forming the first and second numbers as seen in Figures 11.

b. The applicant argues in pages 11-12 for claims that the primary reference by Bhandal fails to disclose the newly added limitations because Bhandal fails to disclose the retrieving a stored value as result of multiplication of first/second plurality of bits wherein the first/second plurality of bits is fewer than the bits of the first/second numbers in page 11 and Bhandal fails to disclose the summing scaled products since Bhandal only discloses sum of the products.

The examiner respectfully submits that Bhandal as primary reference discloses almost all the limitations of the claims, except second product is retrieved from table instead of direct performing multiplication. However, the secondary reference by Schier shows the deficiency of Bhandal by showing the product of numbers can be retrieved by lookup table. Thus, clearly Bhandal clearly shows general concept of supporting the first/second plurality of bits is fewer than the bits of the first/second numbers regardless whether the product is performed directly or looked up. Furthermore, Figures 11 show the summing scaled products as seen in Figure 11B.

c. The applicant argues in pages 12-14 for claims that there is no basis for combining the references.

The examiner respectfully submits that the rejection clearly states the motivation for combining the references and obviously one ordinary skill in the art would known the benefits of having multiplication by retrieving product from table/memory instead of actual performing direct multiplication of product. One

quick lookup at Google produces this link for obvious advantage of having LUT instead direct multiplication at http://www.coranac.com/tonc/text/fixed.htm.

d. The applicant argues in pages 15-16 for claims that the cited references fail to show the limitations of newly added claims 23-24 and further scaling the stored value comprise routing the stored value directly to an adder at inputs of appropriate significance.

The examiner respectfully submits that scaling and routing to appropriate significance or position for summing must be exits in multiplication, otherwise it would produce wrong result of multiplications. Figures 11 show multiple configuration of multiplications wherein the result of certain products are shifted as scaled or routed to correct significance for summing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

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